

Interface card for the latest data formats complements the R&S®UPV audio analyzer

State-of-the-art circuits in multichannel audio systems, wireless communications applications and Bluetooth® components use new data formats to transmit audio content. The top-class R&S®UPV audio analyzer is already well prepared for these formats: Equipped with the new R&S®UPV-B42 universal serial interface, it can adapt virtually all existing audio data formats.

Increasing variety of digital audio interfaces

Nowadays, interconnecting digital audio equipment via standardized interfaces is considered standard procedure. Professional sound studios use the AES/EBU format, while devices for the consumer sector are equipped with electrical or optical interfaces based on the S/P-DIF standard.

However, when looking inside such audio devices, i.e. at the circuitry interconnecting the various modules and components, primarily different serial data interfaces are used. Dual-channel, device-internal audio data transmission often utilizes the inter-IC sound (I²S) bus standard that has been established worldwide. The R&S®UPV has supported this format for quite some time now with the R&S®UPV-B41 I²S interface option.

The compact R&S®UPV audio analyzer easily handles all types of measurements in the audio sector, meeting the extreme demands of both analog technologies and high-resolution digital media (see NEWS from Rohde&Schwarz (2008) No. 196, pp 36–38).

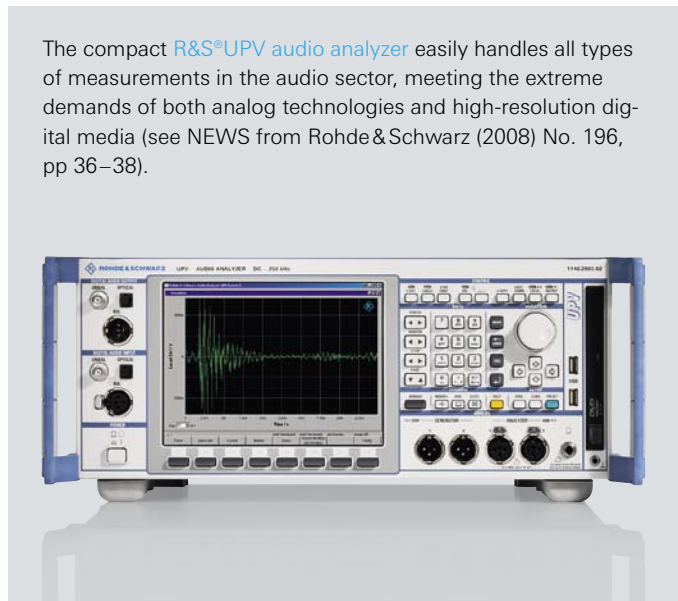
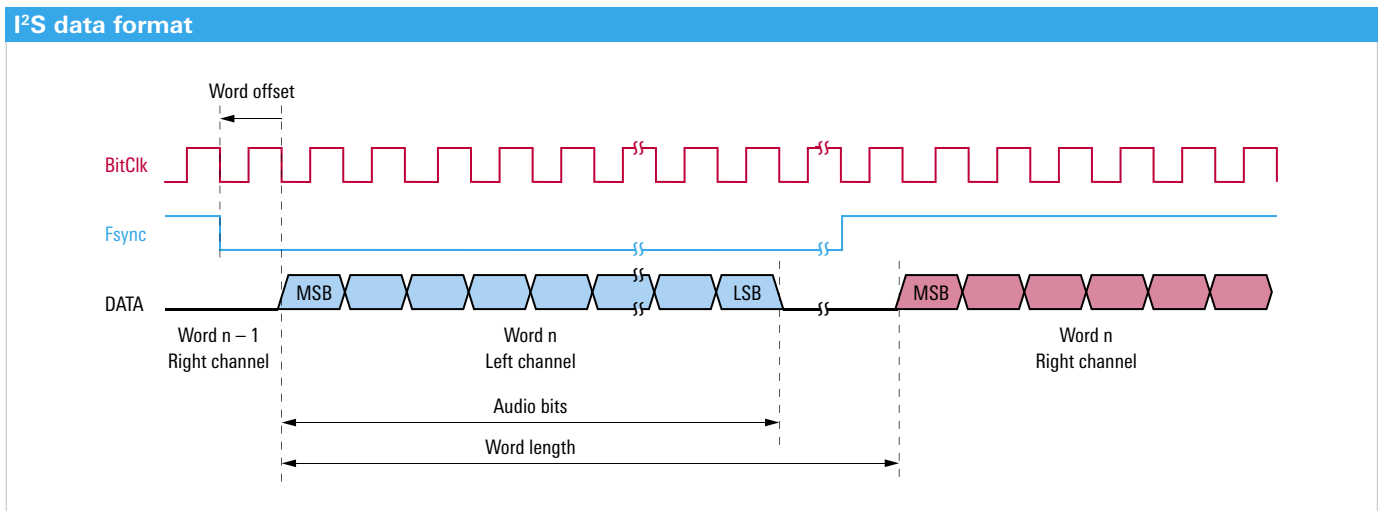


FIG 1 Fundamental signal characteristic of a digital audio transmission in I²S format.



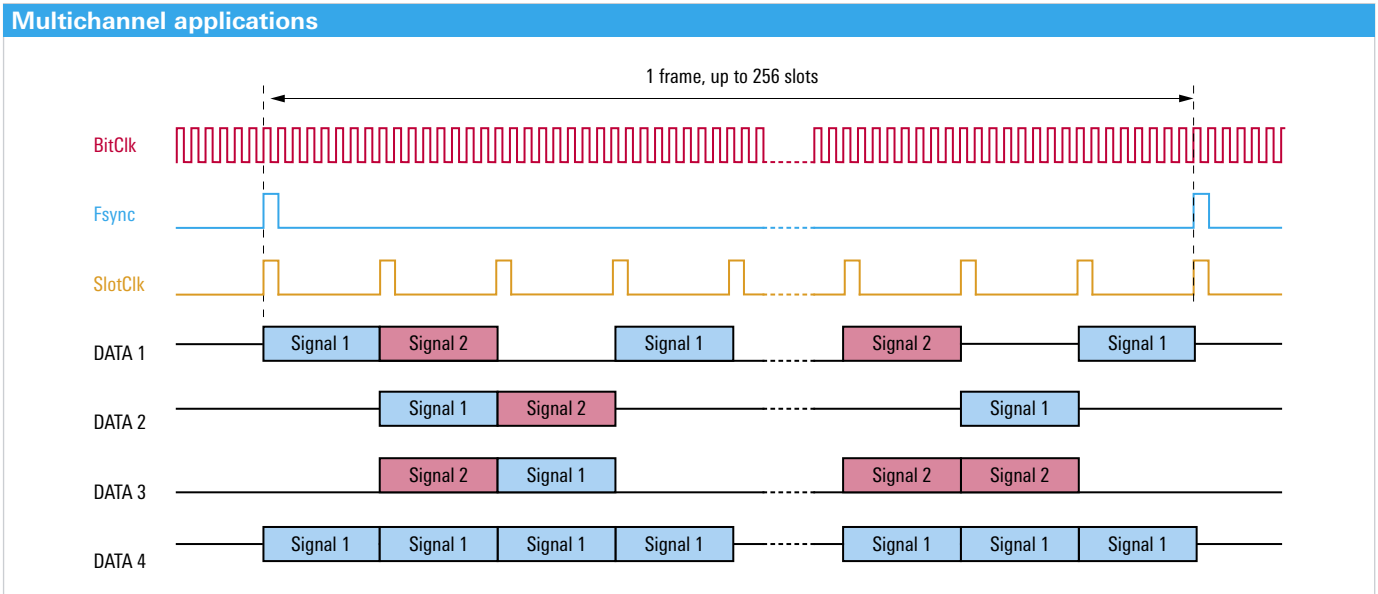


FIG 2 The R&S®UPV-B42 interface card can handle a maximum of 256 slots in up to 4 data lines.

With new applications, however, the limits of the I²S bus have been reached. The widely spread use of surround sound technology, for example, resulted in the development of multichannel A/D and D/A converters. Plus, wireless communications applications and audio transmission in Bluetooth® components demanded new data formats for transmitting audio content.

The new universal serial interface card (R&S®UPV-B42 option) for the R&S®UPV audio analyzer supports all of these developments. Like all other options of the R&S®UPV-B4x series, this interface card is simply plugged into one of the two slots on the rear of the audio analyzer.

The I²S audio format – basis for numerous new developments

The new R&S®UPV-B42 interface card also supports the conventional I²S audio format, which is briefly described below, as many state-of-the-art developments are based on it. Three basic signals are defined with this standard: BitClk (bit clock), Fsync (frame synchronization) and DATA (FIG 1). With each period of the bit clock, one audio data bit is transmitted; DATA is a dual-channel, multiplexed, bit-serial data stream, and Fsync designates the start-of-word in the serial data stream and differentiates between the left and the right channel. Audio data is transmitted using the “MSB first” method in two’s complement format. Common word lengths are 16 bit, 24 bit and 32 bit, but operation with fewer audio bits is also

possible. Generally, the transmit IC generates the clock, frame synchronization and data; in more complex systems, the transmit IC can be synchronized by a central system clock referred to as the master clock.

Further developments in the transmission of serial digital audio data extend and modify many of these parameters, use more channels and higher clock rates, etc. The new R&S®UPV-B42 interface card offers even more functionalities than currently required.

Multichannel applications and variable data formats

Converter ICs for multichannel audio systems are currently available with up to eight serially transmitted audio channels; the telecommunications sector uses systems with even more channels. The new R&S®UPV-B42 option can generate and analyze data streams with up to 256 channels (slots) transmitted in time multiplex. Up to four data lines, each with different data content, can be used (FIG 2). The individual slots can be generated individually with up to two different test signals or with zero signals. In addition, each channel can be switched to high impedance (tristate). The analyzer can simultaneously evaluate up to eight audio data streams that can be selected from among all data lines and slots.

All signals used in digital transmission can be adapted to the task at hand as is shown by FIG 4:

- I BitClk** Can be set to rising or falling slopes.
- I Fsync** In addition to the square wave typically used with I²S (Fsync is set to low during the first half of the word length, and high during the second half), the signal can also be operated with the length of one or more clock periods. Variable offsets allow the Fsync signal to be shifted to any position of the frame. Rising or falling slopes can also be used here.
- I SlotClk** While Fsync defines a signal for each frame, slot clock is an additional line that generates a signal for each slot. SlotClk offers the same setting capabilities as the Fsync signal.
- I DATA** The data lines can be operated in the “MSB first” or “LSB first” formats. The length of the slots can be set from 8 bit up to 256 bit and the slots can be filled with audio data words ranging from 8 bit to 32 bit. Depending on the selected settings, the audio data bits can be preceded by lead bits that have no data content so that the data can be positioned at any point within the frame.

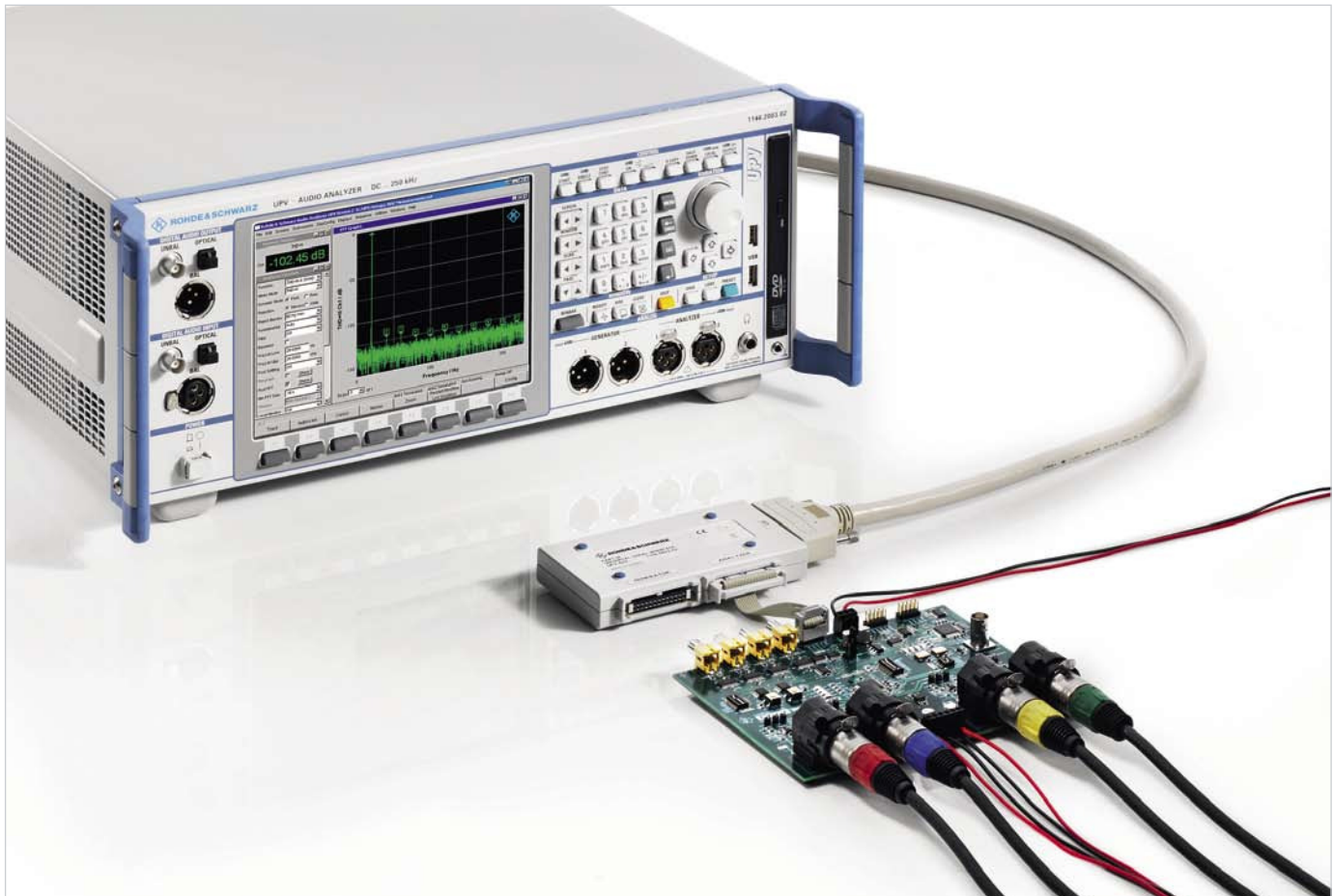
Wide variety of synchronization capabilities and other features

The generator and analyzer of the interface card can each be operated using internal (master) or external (slave) synchronization. Synchronization can be performed via a master clock, Fsync, or both Fsync and BitClk. In complex systems, for example, the central clock can be generated by the R&S®UPV audio analyzer, or the analyzer can be synchronized to external clocks in slave mode.

In special applications, the BitClk signal may not be continuously present. In the gated clock mode, the new R&S®UPV-B42 option also handles this mode in both the generator and the analyzer. For checking the jitter sensitivity of input circuits, the master clock and the Fsync, BitClk and DATA signals can also be output with jitter.

The explanations above clearly show that full utilization of the maximum frame and data lengths results in clock rates that extend well into the MHz range. The option has therefore

FIG 3 Measurement on a multichannel converter: The probe for the new interface card helps to avoid reflections by enabling short connections to the DUT.



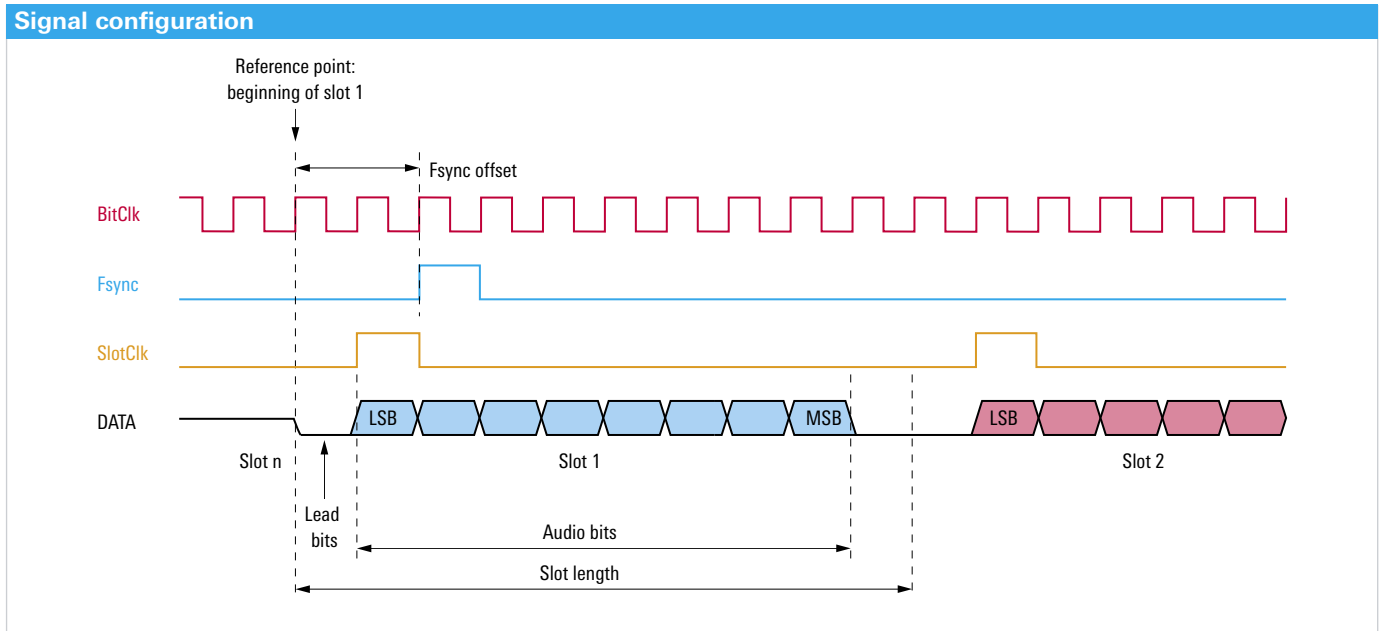


FIG 4 Versatile signal settings for digital data transmission.

been equipped with a probe that can be used to establish short and therefore low-reflection connections to the circuits to be analyzed (FIG 3). All logic families from 3.3 V down to 0.9 V can be connected.

The generator and the analyzer of the interface card can be configured independently of each other, allowing the evaluation of components and modules with different input and output formats. And the generator and analyzer can also be used together with the other interfaces of the R&S®UPV audio analyzer. For measurements on eight-channel D/A converters, for example, the new option can be combined with another new option, the R&S®UPV-B48 eight-channel analog inputs card [*].

This article describes only some of the many configurations that are possible with the new R&S®UPV option. Further information on the data formats required for special applications can be found in the R&S®UPV-B42 data sheet.

Summary

The new R&S®UPV-B42 universal serial interface provides digital audio interfaces, allowing extremely versatile adaptation to almost any audio circuit. Up to eight digital audio signals can be measured simultaneously. Like all options of the R&S®UPV-B4x family, this option can be retrofitted by the customer and installed in existing devices.

Klaus Schiffner

Condensed data of the R&S®UPV with the R&S®UPV-B42 option

Input/output voltages	for 0.9 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V logic families
Data format	linear PCM, A-law, μ -law
Frame synchronization frequency	0.85 kHz to 400 kHz
Number of slots per frame	1 to 256
Frame synchronization slope	rising or falling
Slot length	8 bit to 256 bit
Audio bits	8 to 32
Audio bit sequence	MSB first or LSB first
Bit clock slope	rising or falling
Bit clock frequency	up to 55 MHz
Master clock frequency	up to 110 MHz

References

- * Audio analysis in production: saving time with 16 measurement channels. News from Rohde&Schwarz (2008) No. 196, pp 36–38.